REMARKS

Claim 69 has been canceled. Claims 1-30 and 36-68 are pending in the present application. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

Claims 1-44, 50-59 and 65-72 stand rejected under 35 U.S.C. § 102 (e) as being anticipated by Perino et al., US Patent No. 6,545,875 (hereinafter "Perino"). The rejection is respectfully traversed and reconsideration is respectfully requested.

On September 12, 2003 Applicant submitted a "Declaration Of Terry R. Lee Under 37 CFR 1.131" and on February 4, 2004 Applicant submitted a "Supplemental Declaration Of Terry R. Lee Under 37 CFR 1.131" (hereinafter the "Lee Declarations"); Terry R. Lee is the inventor of the claimed inventions.

The Lee Declarations establish a "prior invention" with respect to the effective date of the Perino reference (i.e., May 10, 2000). That is, the Lee Declarations establish conception of the claimed inventions prior to the effective date of the Perino reference (i.e., May 10, 2000) coupled with due diligence from prior to the reference date to the filing date of the present application (i.e., May 31, 2000). See M.P.E.P. § 715.07. "A rejection based on 35 U.S.C. 102(e) can be overcome by . . . [f]iling an affidavit or declaration under 37 CFR 1.131 showing prior invention." M.P.E.P § 706.02(b). As such, Applicant respectfully submits that claims 1-44, 50-59 and 65-72 are allowable over Perino.

The Office Action, however, has stated that the Lee Declarations are ineffective to overcome the Perino reference because allegedly the Perino reference and the present application claim the same patentable invention. Applicant's representative had a telephone conversation with Examiner Huynh on May 6, 2004. During the call,

the Examiner suggested that the Lee Declarations would be effective if the claims of the present application were amended to be different than the claims in the Perino reference. Applicant's representative gratefully appreciates the courtesy shown by the Examiner during the conversation.

Applicants respectfully submit that, for the reasons set forth below, the Perino reference and the present application are already claiming different inventions. As such, the Lee declarations should be effective in overcoming the rejections based on Perino.

Initially, Applicant respectfully submits that claims 1-29 of the present application are method claims. Perino does not include any method claims and as such, the present application and Perino cannot be claiming the same patentable invention recited in claims 1-29 of the present application.

Moreover, Applicant respectfully submits that claims 36-65 of the present application are "bus system" claims. Perino does not include any "bus system" claims and as such, the present application and Perino cannot be claiming the same patentable invention recited in claims 36-65 of the present application.

Similarly, Applicant respectfully submits that claims 66-68 of the present application are "processor-based system" claims. Perino does not include any "processor-based system" claims and as such, the present application and Perino cannot be claiming the same patentable invention recited in claims 66-68 of the present application.

Moreover, as shown below, each independent claim of the Perino patent contains at least one element that is not disclosed in the present application. As such,

each claim of the Perino patent contains at least one element that is not claimed in the present application.

Independent claims 1 and 7 of Perino coincides with the following Figure reproduced from Perino:

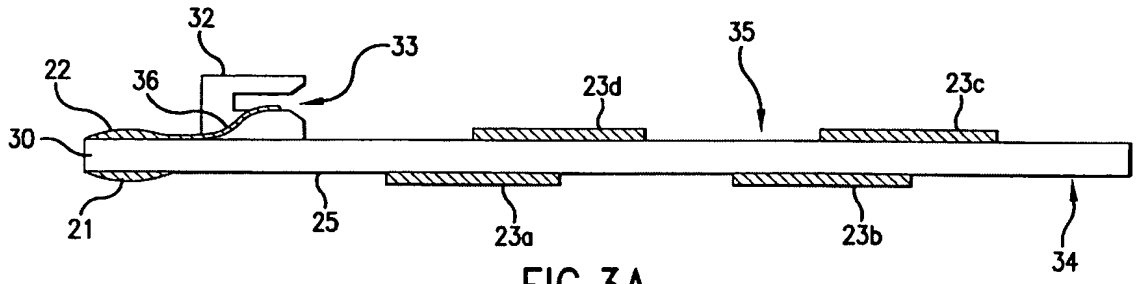


FIG.3A

The following table illustrates the elements of Perino's claims 1 and 7 that are not being claimed or disclosed in the present application.

Claim 1 of Perino	**Present Application**
a first set of edge fingers [21] disposed at the first end and on the first surface of the PCB;	There are no claims in the present application directed to a first set of edge fingers. In addition, the present application does not disclose a first set of edge fingers.
a second set of edge fingers [22] disposed at the first end and on the second surface of the PCB;	There are no claims (or disclosure) in the present application directed to a second set of edge fingers. Moreover, there are no claims and no disclosure to a second set of edge fingers on the same end as a first set of edge fingers.
an internal bus extending from the first set	There are no claims, or disclosure, in the

of edge fingers, substantially traversing the length of the first surface, folding back proximate the second end, substantially traversing the length of the second surface, and terminating at the second set of edge fingers; and,	present application to an internal bus extending from the first set of edge fingers, substantially traversing the length of the first surface, folding back proximate the second end, substantially traversing the length of the second surface, and terminating at the second set of edge fingers.
a right-angle connector [32] mounted on at least one of the first and second surfaces, and mounted proximate the first end, and adapted to mechanically receive and electrically connect another module.	There are no claims, or disclosure, in the present application of a right angle connector.

Claim 7 of Perino	**Present Application**
a set of edge fingers [21] disposed at the first end of the PCB and mounted on either the top surface or bottom surface of the PCB;	There are no claims, or disclosure, in the present application directed to a first set of edge fingers.
a right-angle connector [32] adapted to mechanically receive and electrically connect another module, the right-angle connector being mounted on either the bottom surface or top surface of the PCB opposite the surface on which the set of edge fingers are disposed and mounted proximate the second end of the PCB; and	There are no claims, or disclosure, in the present application of a right angle connector.
an internal bus extending from the set of edge fingers, substantially traversing the length of the module, and terminating at the right-angle connector.	There are no claims, or disclosure, in the present application of a bus connected to a right angle connector.

Claim 13 of Perino coincides with the following Figure reproduced from Perino:

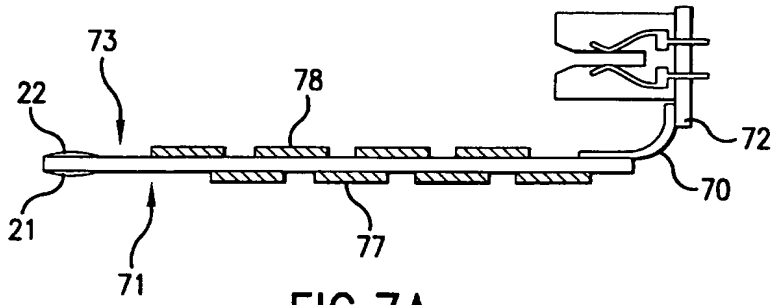


FIG.7A

The following table illustrates the elements of Perino's claim 13 that are not being claimed or disclosed in the present application.

Claim 13 of Perino	**Present Application**
a first set of edge fingers [21] disposed on the first primary edge between first and second ends and on the first surface of the PCB;	There are no claims, or disclosure, in the present application directed to a first set of edge fingers.
a second set of edge fingers [22] disposed on the first primary edge between first and second ends and on the second surface of the PCB, wherein the first and second set of edge fingers are adapted to connect with an electrical connector associated with another module or a motherboard; and,	There are no claims, or disclosure, in the present application directed to a second set of edge fingers on the same edge as a first set of edge fingers.
an internal bus comprising a plurality of signal lines running from at least one of the first and second set of edge fingers to a connector [70/72] disposed on the second primary edge of the PCB between the first and second ends.	There are no claims, or disclosure, in the present application directed to a bus connected to edge fingers on one edge and a connector on another edge.

Claim 18 of Perino coincides with the following Figure reproduced from Perino:

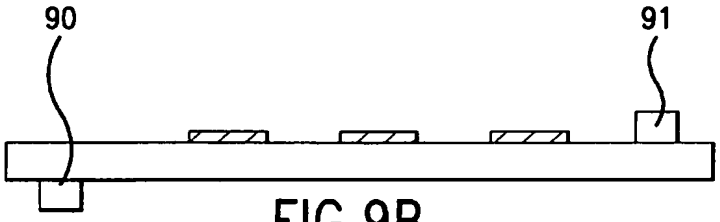


FIG.9B

The following table illustrates the elements from Perino's claim 18 that are not being claimed or disclosed in the present application.

Claim 18 of Perino	**Present Application**
an internal bus laterally traversing the one or more rows, the internal bus running from a first connector [90] disposed on the first primary surface proximate the first end to a second connector [91] disposed on the second primary surface proximate the second end;	There are no claims, or disclosure, in the present application for a bus routed between a first connector on a first surface at a first end of a card to a second connector on a second surface at a second end of a card.
wherein the at least one of the first and second connectors [90, 91] is adapted to mechanically support and electrically connect another module.	There is no claim to this element and there is no corresponding disclosure in the present application.

Claim 19 of Perino coincides with the following Figure reproduced from Perino:

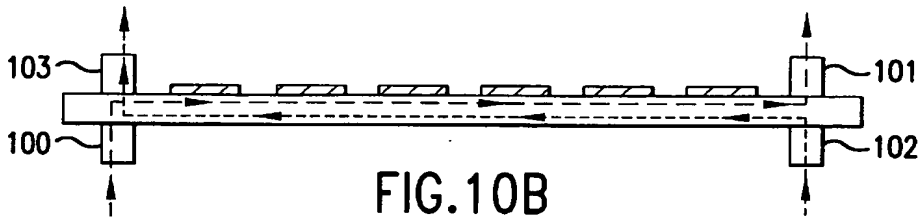


FIG.10B

The following table illustrates the elements from Perino's claim 19 that are not being claimed or disclosed in the present application.

Claim 19 of the '875 Patent	**Present Application**
a first internal bus laterally traversing the one or more rows in a first direction, the first internal bus running from a first connector [100] disposed on the first primary surface proximate the first end to a second connector [101] disposed on the second primary surface proximate the second end;	There are no claims, or disclosure, in the present application for a bus routed between a first connector on a first surface at a first end of a card to a second connector on a second surface at a second end of a card.
a second internal bus laterally traversing the one or more rows in a second direction opposite the first direction, the second internal bus running from a third connector [102] disposed on the first primary surface proximate the second end to a fourth connector [103] disposed on the second primary surface proximate the first end;	There are no claims, or disclosure, in the present application for a second bus routed between a third connector and a fourth second connector.
wherein at least one of the first, second, third and fourth connectors [100, 101, 102, 103] is adapted to mechanically support and electrically connect another module.	There are no claims to this element and there is no corresponding disclosure of this element in the present application.

Claim 20 of Perino coincides with the following Figure reproduced from Perino:

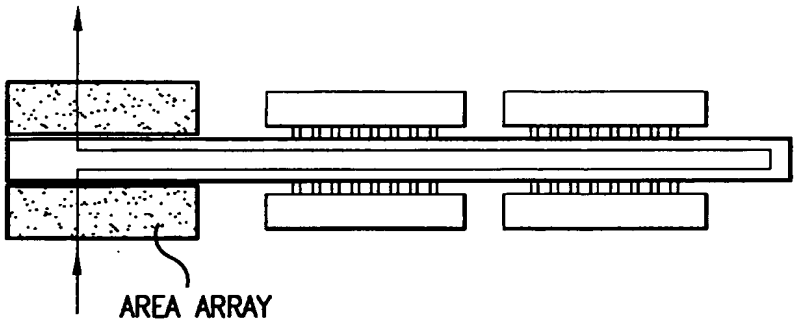


FIG.11B

The following table illustrates the elements from Perino's claim 20 that are not being claimed or disclosed in the present application.

Claim 20 of Perino	**Present Application**
a plurality of N first connectors disposed on the first primary surface proximate the first edge, each one of the plurality of N first connectors being substantially aligned with one of the N columns;	In the present application there are no claims to, and no disclosure of, a plurality of N first connectors disposed on the first primary surface proximate the first edge, each one of the plurality of N first connectors being substantially aligned with one of the N columns.
a plurality of N second connectors disposed on the second primary surface proximate the first edge, each one of the plurality of N second connectors being substantially aligned with one of the N columns;	In the present application there no claims to, and no disclosure of, a plurality of N second connectors disposed on the second primary surface proximate the first edge, each one of the plurality of N second connectors being substantially aligned with one of the N columns.
an internal bus comprising N bus portions, each one of the N bus portions extending from a respective one of the plurality of first connectors, substantially traversing the breadth of the PCB from	In the present application there are no claims to, and no disclosure of, an internal bus comprising N bus portions, each one of the N bus portions extending from a respective one of the plurality of first

first primary edge to the second primary edge, folding back at the second primary edge, substantially traversing the breadth of the PCB from second primary edge to the first primary edge, and terminating at a respective one of the plurality of second connectors;	connectors, substantially traversing the breadth of the PCB from first primary edge to the second primary edge, folding back at the second primary edge, substantially traversing the breadth of the PCB from second primary edge to the first primary edge, and terminating at a respective one of the plurality of second connectors.
wherein the N channel module is mechanically stacked and electrically connected within a bus system comprising a plurality of modules by operation of the first and second connectors.	There is no claim to this element and there is no corresponding disclosure either in the present application.

Claim 21 of Perino coincides with the following Figures reproduced from Perino:

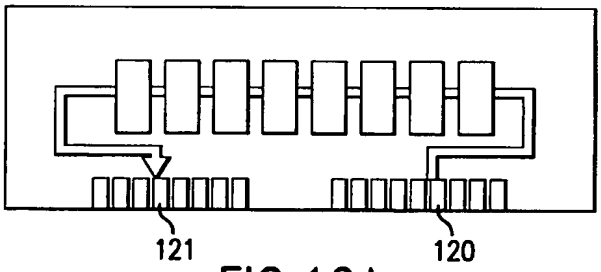


FIG.12A

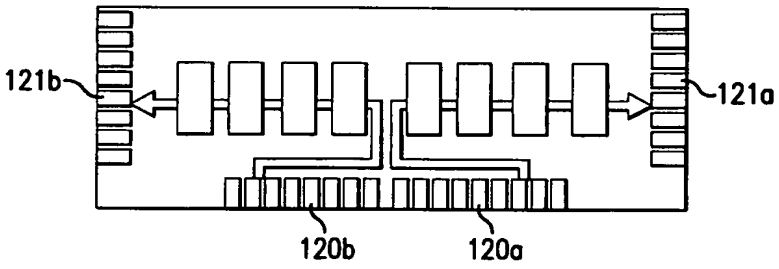


FIG.12B

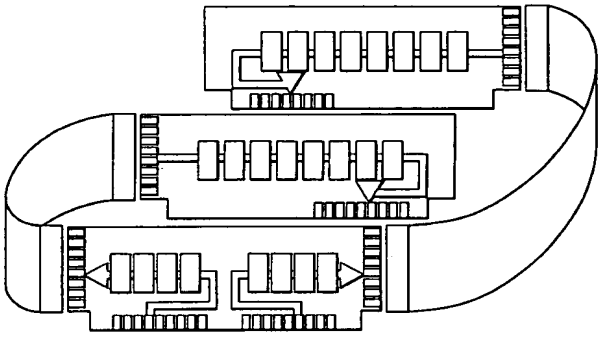


FIG.13C

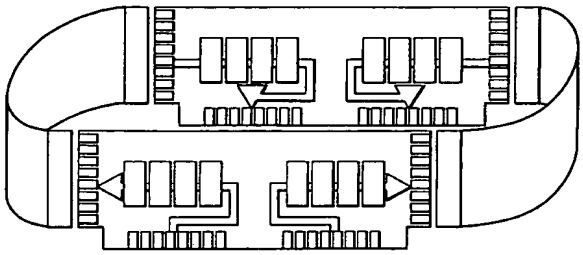


FIG.14A

The following table illustrates the elements from Perino's claim 21 that are not being claimed in the present application.

Claim 21 of Perino	**Present Application**
at least one set of input finger connectors [121] disposed on the first primary edge and adapted for connection to a corresponding electrical connector;	In the present application, there are no claims to at least one set of input finger connectors disposed on the first primary edge and adapted for connection to a corresponding electrical connector.
at least one set of output finger connectors [120] disposed on one of the first primary edge, the second primary edge, the first lateral edge, or the second lateral edge, and adapted for connection to a corresponding electrical connector; and,	In the present application, there are no claims to at least one set of output finger connectors disposed on one of the first primary edge, the second primary edge, the first lateral edge, or the second lateral edge, and adapted for connection to a corresponding electrical connector.
an internal bus forming a plurality of signal paths between the at least one set of input finger connectors [121] and the at last one set of output finger connectors [120], and connected to at least one of the plurality of ICs.	In the present application, there are no claims to an internal bus forming a plurality of signal paths between the at least one set of input finger connectors and the at last one set of output finger connectors, and connected to at least one of the plurality of ICs.

Claim 25 of Perino coincides with the following Figure reproduced from Perino:

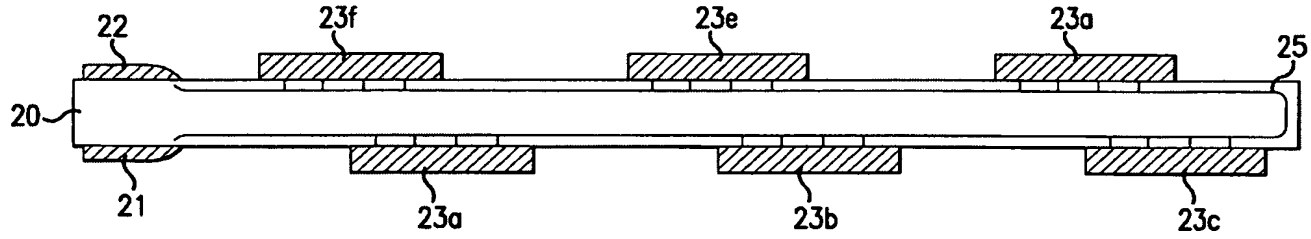


FIG.2

The following table illustrates the elements from Perino's claim 21 that are not being claimed or disclosed in the present application.

Claim 25 of Perino	**Present Application**
a first set of edge fingers [21] disposed at the first end and on the first surface of the PCB;	There are no claims, or disclosure, in the present application directed to a first set of edge fingers.
a second set of edge fingers [22] disposed at the first end and on the second surface of the PCB;	There are no claims, or disclosure, in the present application directed to a second set of edge fingers disposed at the first end (i.e., same end as the first set of fingers) and on the second surface of the PCB.
an internal bus extending from the first set of edge fingers, substantially traversing the length of the first surface, folding back proximate the second end, substantially traversing the length of the second surface, and terminating at the second set of edge fingers.	In the present application, there are no claims to, or disclosure of, extending from the first set of edge fingers, substantially traversing the length of the first surface, folding back proximate the second end, substantially traversing the length of the second surface, and terminating at the second set of edge fingers.

As shown above, Perino and the present application are not claiming the same patentable invention. The Lee Declarations should be effective and the rejection under Perino withdrawn.

Furthermore, Applicant respectfully wishes to point out that if the rejection under Perino is maintained, Applicant's lone remedy will be to file an Interference. In order for an interference in fact to exist, however, Perino and the present application would have to be claiming the same patentable invention. 37 C.F.R. § 1.601(j). As set forth above, this is not the case and an interference in fact does not exist.

The claims of the Perino reference are directed to several very specific species of Applicant's generic invention. According to the Court of Appeals for the Federal Circuit ("CAFC"), under the "two-way" analysis, the claims of a senior party are analyzed in view of the claims of a junior party as if the junior party's claims were prior art, and vice versa. If in either analysis, one set of claims is determined to be patentable over the other set, there is no interference-in-fact because the claims are considered to cover separate patentable inventions. Eli Lilly & Co. v. Bd. of Regents of the Univ. of Wash., 334 F.3d 1264, 1268 (Fed. Cir. 2003). Only if *both* inventions anticipate or render each other obvious are the two inventions considered to be the "same patentable invention," which would allow the interference to continue. Id. at 1268-69. This applies even when the Senior party is claiming a species of the Junior party's genus. Id. This is the situation we have here. As shown above, there is no interference in fact between the pending claims of the present application and Perino.

Claims 30-35 and 69-72 are canceled.

For at least the reasons set forth above, the rejection of claims 1-29, 36-44, 50-59 and 65-68 should be withdrawn and all of the claims allowed.

Claims 45 and 60 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino in view of Cargin, Jr. et al., US. Patent. No. 6,023,147, (hereinafter "Cargin"). The rejection is respectfully traversed and reconsideration is respectfully requested.

As noted above, the Lee Declarations establish a completion of the claimed inventions prior to the effective date of the Perino reference. "Applicant may overcome a 35 U.S.C. 103(a) rejection based on a combination of references by showing completion of the invention by applicant prior to the effective date of any of the references." M.P.E.P. § 715.02. Since Applicant has established a completion of the claimed inventions prior to the effective date of the Perino reference, and Cargin does not teach or suggest any of the features of the claimed inventions, Applicant respectfully submits that claims 45 and 60 are allowable over the cited combination. Accordingly, for at least the reasons set forth above, the rejection of claims 45 and 60 should be withdrawn and all of the claims allowed.

Claims 46-49 and 61-64 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perino in view of the Handbook of LAN Cable Testing (hereinafter the "Handbook"). The rejection is respectfully traversed and reconsideration is respectfully requested.

As noted above, the Lee Declarations establish a completion of the claimed inventions prior to the effective date of the Perino reference. "Applicant may overcome a 35 U.S.C. 103(a) rejection based on a combination of references by showing completion of the invention by applicant prior to the effective date of any of the references." M.P.E.P. § 715.02. Since Applicant has established a completion of the claimed inventions prior to the effective date of the Perino reference, and the Handbook does not teach or suggest any of the features of the claimed inventions, Applicant

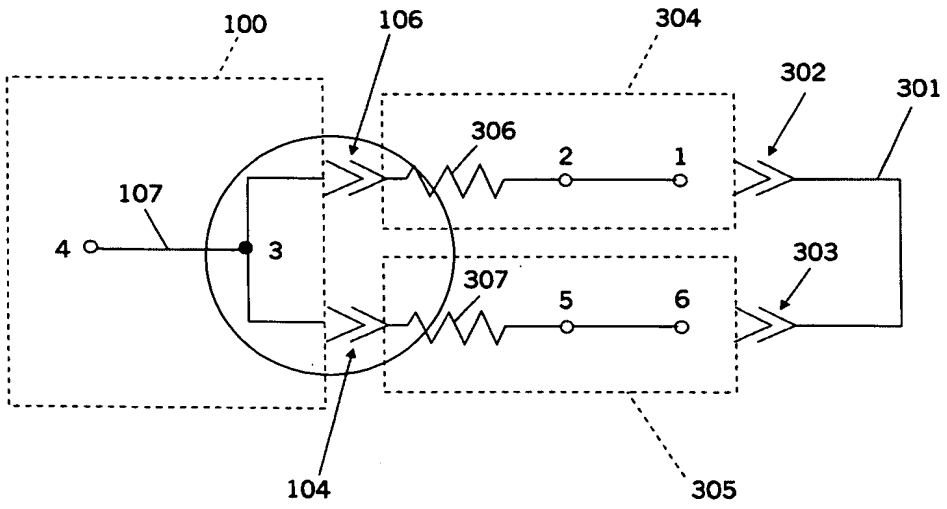
respectfully submits that claims 46-49 and 61-64 are allowable over the cited combination. Accordingly, for at least that reason, withdrawal of the rejection of claims 61-64 is respectfully requested.

Claims 1, 4-14, 17-30, 33-36, 39-44, 50-51, 54-59, and 65-72 stand rejected under 35 U.S.C. § 102 (e) as being anticipated by Appel et al., U.S. Patent No. 6,219, 733 ("Appel"). Reconsideration is respectfully requested.

Claim 1 recites a method of routing a system bus to a plurality of expansion cards comprising, "routing the bus into a first connector and into a first circuit card residing within the first connector; routing the bus from a portion of the first circuit card into a portion of a second circuit card residing within a second connector, wherein the bus is routed from the first circuit card to the second circuit card without entering the second connector; and routing the bus through the second circuit card to the second connector."

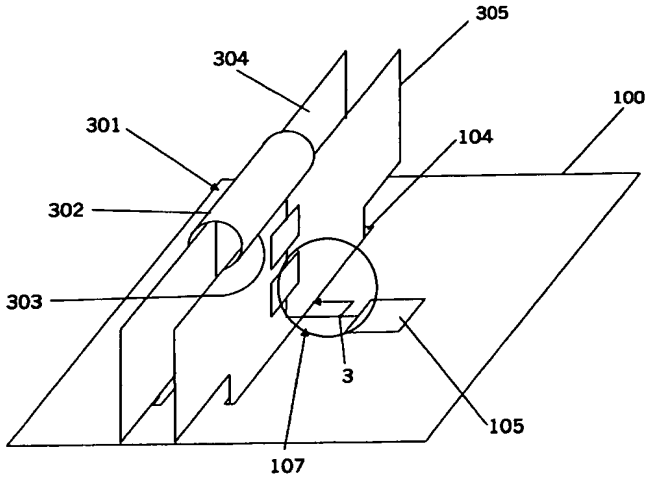
Applicant respectfully submits that Appel fails to disclose, teach or suggest the claimed invention because Appel routes its bus 107 (described as a net) on its motherboard (board 100) and between its connectors 104, 106 as shown on the next page:

FIG. 3



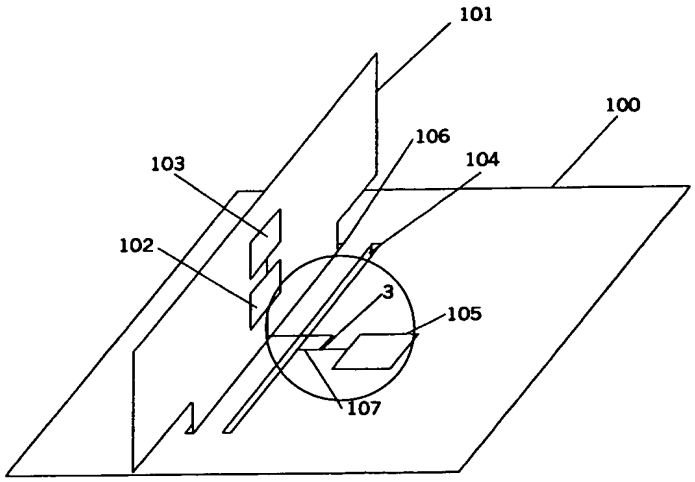
Appel discloses daughter boards 304, 305 connected to the motherboard 100 through the connectors 104, 106. In addition, a connector 301 connects the top of the two daughter boards 304, 305. According to the specification, Appel "utilizes a cable connector 301 on top of daughter cards 304 and 305 to interconnect the data lines across the two cards. This forms a loop with a stub between nodes 3 and 4. The stub is part of the net 107 on the system board 100." Appel Col. 3, lines 62-67 (emphasis added). As can be seen from the reproduced figures, the "loop" includes routing the bus/net 107 on the motherboard 100 through the connectors 104, 106 (see circled portions). Figure 4 of Appel is reproduced on the next page.

FIG. 4



Furthermore, Appel makes it clear that the bus/net 7 is routed through the connectors 104, 106 since "the present invention does not result in any modifications needed to the system board 100." Appel, Col. 4, lines 18-20. The prior art board 100 reproduced on the next page clearly shows the bus/net 7 being routed through the connectors 104, 106 on the motherboard 100.

FIG. 1
PRIOR ART



As such, Appel fails to disclose, teach or suggest a "method of routing a system bus to a plurality of expansion cards" where the bus is routed "into a first connector and into a first circuit card residing within the first connector" and where the "bus is routed from the first circuit card to the second circuit card without entering the second connector." Accordingly, for at least the foregoing reasons, claim 1 is allowable over Appel.

Claims 4-13 depend from claim 1 and are allowable along with claim 1 for at least the reasons set forth above and on their own merits.

Claim 14 recites "routing the bus into a first circuit card residing within a first slot; routing the bus from a portion of the first circuit card into a portion of a second circuit card residing within a second slot, wherein the bus is routed from the first circuit card to the second circuit card without entering the second slot; and routing the bus through the second circuit card." As set forth above, Appel fails to disclose, teach or suggest the claimed invention. Claims 17-29 depend from claim 14 are allowable along with claim 14 for at least the reasons set forth above and on their own merits.

Claim 36 recites "wherein said bus is routed into a first connector, into a first circuit card residing within said first connector, out of a portion of said first circuit card into a portion of a second circuit card residing within a second connector and through said second circuit card, and wherein said bus is routed from said first circuit card to said second circuit card without entering said second connector." As set forth above, Appel fails to disclose, teach or suggest the claimed invention. Claims 39-44 and 50 depend from claim 36 are allowable along with claim 36 for at least the reasons set forth above and on their own merits.

Claim 51 recites "wherein said bus is routed into a first circuit card residing within a first slot, out of a portion of said first circuit card and into a portion of a second circuit card residing within a second slot and out of the second circuit card, wherein said bus is routed from said first circuit card to said second circuit card without entering said second slot." As set forth above, Appel fails to disclose, teach or suggest the claimed invention. Claims 54-59 and 65 depend from claim 51 are allowable along with claim 51 for at least the reasons set forth above and on their own merits.

Claim 66 recite "wherein said bus is routed into a first connector, into a first circuit card residing within said first connector, out of a portion of said first circuit card into a portion of a second circuit card residing within a second connector, through said second circuit card and out of said second connector, wherein said bus is routed from said first circuit card into said second circuit card without entering said second connector." Claim 67 recites "wherein said bus is routed into a first circuit card residing within a first slot, out of a portion of said first circuit card and into a portion of a second circuit card residing within a second slot and out of the second circuit card, wherein said bus is routed from said first circuit card into said second circuit card without entering said second slot." Claim 68 recites "wherein said bus is routed into a first memory circuit card residing within a first slot, out of a portion of said first memory circuit card and into a portion of a second memory circuit card residing within a second slot, and out of the second memory circuit card, wherein said bus is routed from said first memory circuit card into said second memory circuit card without entering said second slot." For at least the reasons set forth above, Appel fails to disclose, teach or suggest the claimed inventions. As such, claims 66-68 are allowable over Appel.

Claims 30-35 and 69-72 are canceled.

The rejection should be withdrawn and claims 1, 4-14, 17-29, 36, 39-44, 50, 51, 54-59 and 65-68 allowed.

Claims 2-3, 15-16, 31-32, 37-38, and 52-53 stand rejected under 35 U.S.C. § 103(a) as being obvious over Appel. Reconsideration is respectfully requested.

Claims 2-3 depend from claim 1 and are allowable along with claim 1 for at least the reasons argued above and on their own merits. Claims 15- 16 depend from claim 14, and are allowable along with claim 14 for at least the reasons argued above and on their own merits.

Claims 31- 32 have been previously canceled.

Claims 37-38 depend from claim 36 and are allowable along with claim 36 for at least the reasons argued above and on their own merits.

Claims 52-53 depend from claim 51 and are allowable along with claim 51 for at least the reasons argued above and on their own merits.

The rejection should be withdrawn and claims 2-3, 15-16, 37-38 and 52-53 allowed.

Claims 45 and 60 stand rejected under 35 U.S.C. § 103(a) as being obvious over Appel in view of Cargin. Reconsideration is respectfully requested.

Cargin discloses a hand held computer apparatus that includes a ribbon cable for coupling a radio module to a controller card. Claim 45 depends from claim 36 and are allowable along with claim 36 for at least the reasons argued above and on their own merits. Claim 60 depends from claim 51 and are allowable along with claim 51 for

at least the reasons argued above and on their own merits. Accordingly, the rejection should be withdrawn and claims 45 and 60 allowed.

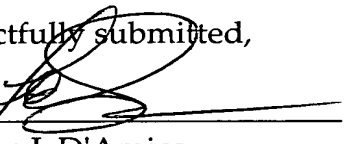
Claims 46-49 and 61-64 stand rejected under 35 U.S.C. § 103(a) as being obvious over Appel in view of the Handbook. Reconsideration is respectfully requested.

The Handbook discloses different types of data cables. Claims 46-49 depend from claim 36 and are allowable along with claim 36 for at least the reasons argued above and on their own merits. Claims 61-64 depend from claim 51 and are allowable along with claim 51 for at least the reasons argued above and on their own merits. Accordingly, the rejection should be withdrawn and claims 46-49 and 61-64 allowed.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: July 19, 2004

Respectfully submitted,

By 

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